REMARKS

Applicants respectfully traverse and request reconsideration.

As a preliminary matter, Applicants wish to thank the Examiner for the Notice that claims 2-13 and 22-23 have been allowed.

Remaining claims 14-17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Cheney et al. in view of Adams et al. As to claim 14, in the "Response to Arguments" section of the Office Action, the examiner states that the step of "generating a secondary set of control signals from the compressed transport stream control signals" is met by the frame buffer pointer control 686 that generates additional control signals citing col. 9, lines 31 through col. 10 line 41. Applicants have amended the claim to point out that among other things, the claim requires storing at least a portion of the compressed transport stream data signals, via a first bus, and a memory buffer controlled by the secondary set of control signals and sending the contents of the memory buffer, via the first bus, to a system bus. Applicants respectfully submit that such an operation is not taught or suggested by the Cheney reference.

For example, the frame buffer pointer control 686, as noted for example in col. 10, lines 37-42 controls the addresses to the frame buffer storage 653. In fact, the frame buffer pointer control controls rotation of the frame buffers such as frame buffer assignments when in a normal video mode and video scaling mode in accordance with the Cheney description. As such, the frame buffer pointer control 686 is controlled based on the display mode switch logic 696, a video display unit 690. (See for example col. 10, lines 62-67). As such, in a normal display mode, full size scan lines are retrieved from the frame buffer storage and alternatively when in video scaling mode, decoded video that includes scaled scan lines are retrieved from the frame buffer storage and fed directly to the scan line video buffer 684. (See for example col. 10, lines 42-54). As such, the control signals generated, apparently by the frame buffer pointer control 686, actually appear to control based on the type of display mode that has been selected via the display mode switch logic 696 and not from the compressed transport stream control signals as noted in the claim. Accordingly, it appears that the claims are allowable at least for this reason.

Moreover, as claimed, the compressed transport stream 15 stored in the memory buffer via a first bus and then contents of that memory buffer are sent to a system bus via the first bus.

The Cheney reference does not appear to teach such an operation as the bus used to communicate from the memory control unit 652 to the SD RAM 653 is not used to send the contents to the system bus such as the PCI bus shown in FIG. 2. For example the compressed information that is stored in the DRAM 53 only appears to be decoded in video decoder 54 and subsequently displayed via box 58. The contents of the memory DRAM 53 do not appear to be described as being communicated out the PCI bus as the decoder 40 is a self contained video decoder and display chip. As such, Applicants agree that Cheney does not teach this limitation. The Office Action cites Adams as allegedly teaching this limitation. The Office Action alleges that the Adams reference teaches that since the system bus 52 is bi-directional that it teaches the claimed operation. However, Applicants respectfully request a showing as to the precise teaching of Applicants claimed invention as although a bi-directional bus may be shown in Adams, the information communicated over that bus does not appear to be described as including the compressed transport stream data signals from a memory buffer that go by a secondary set of control signals that are also based on the compressed transport stream as required by the claim. Accordingly, Applicants respectfully submit that this claim is also in condition for allowance.

As to dependent claims 15-17, Applicants respectfully reassert the relevant remarks made from the previous response.

Claims 18-20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Schindler. In particular, the implementation of FIG. 5 of Schindler has been cited as including everything in the system claim 18 except for a tuner that receives a digital video broadcast signal and to provide an analog output signal. The Office Action takes official notice that it would have been obvious to one of ordinary skill in the art to have modified the system of Schindler to include a tuner for digital video broadcast signals. However, in the Office Action it does not indicate where such motivation would come from. The alleged motivation appears to be that one of ordinary skill in the art would have modified Schindler to include this operation and structure for the advantage of reducing hardware components in simplifying the system in bypassing the PCI bus. However, Applicants respectfully submit that Schindler teaches away from such a structure since the PCI bus is the only way that Schindler contemplated that the MPEG video streams are received by the video graphics adapter card. In fact, it appears that Schindler teaches

the same prior art system Applicants describe with respect to FIG. 1 in their "Background of the Invention" section of the specification.

As a preliminary matter, Applicants also note that the Office Action alleges that the claimed video graphics adapter is met by the card 318 shown in FIG. 5 of Schindler. However, Applicants respectfully submit that they are not claiming a video graphics adapter card as the claim does not state that it is an entire printed circuit board card. To the contrary, Applicants claim a video graphics adapter. It is known in the art this may be for example an integrated circuit chip. Moreover, a video graphics adapter as claimed is separate from the entire card (but may be employed for example on a card or on any other suitable structure) as noted for example, with respect to FIG. 3 wherein Applicants specification describes the video graphics adapter as having an internal bus and in one embodiment is connected with an internal graphics memory 330 and includes internal graphics engine 320 along with an internal PCI interface that connects to a PCI bus. Accordingly, Applicants respectfully submit that the card 318 is not equivalent to the claimed video graphics adapter. Accordingly, the claims are in condition for allowance.

In any event, as noted above the Schindler reference appears to merely teach what Applicants described as the prior art of FIG. 1 wherein a PCI bus is required to communicate MPEG information to a video graphics adapter. It is noted in Applicant's specification, that one problem that may result in such a structure is that it can be necessary for separate printed circuit boards (cards) to be used to implement the transport stream converter and video adapter. (See for example Specification lines 20-21, page 2). Moreover, Schindler includes a single port that receives a standard cable and has a conventional cable tuner. A PCI bus is necessary for the communication of an MPEG stream from some other source. Applicants claim a different structure. For example, Applicants claim, among other things, that in addition to the digital video broadcast signal tuner, being input in the system, that the video graphics adapter has a transport stream port that receives the compressed transport stream and another data stream. The controller 510 is not a transport stream port, but to the contrary is a controller that receives the MPEG stream through a system bus 312 such as a PCI bus. Applicants claim a video graphics adapter that not only includes the bus interface port bus also a transport stream port to which the received compressed transport stream and another data stream may be received. In addition, the video graphics adapter also includes a graphics engine and a video output port. As such, there is

no transport stream from a digital video broadcast signal from a tuner from a video graphics adapter that has a transport stream port (such as capture block 310) that receives the compressed transport stream and another data stream as claimed. Accordingly, the claims are believed to be in condition for allowance.

As to claim 19 Applicants also amended this claim to note that the memory is an internal memory within the video graphics adapter and that the internal memory is coupled to the graphics engine, the transport stream port and to the bus interface port and stores at least a portion of the compressed transport stream and is also coupled to store data for the graphics engine. As noted for example in the specification on page 6, lines 10-16, different types of digital video data can be received and the reuse of common circuitry can be accomplished. The PCI interface already residing within a video graphics adapter can be used to store transport buffered stream data wherein the internal memory for example stores both compressed data buffered from the transport stream as well as data used by the graphics engine. (See for example page 5, lines 16-20). As such, the graphics memory can operate as a frame buffer for the graphics engine or as a buffer to store the transport stream data. The bus interface port provides an interface between the internal bus to an external system bus, such as a PCI bus or any other suitable bus. Such a bus and memory structure in video graphics adapter is not taught or suggested by the cited reference. Accordingly, this claim is also believed to be in condition for allowance.

As to claim 20 Applicant respectfully reasserts the relevant remarks made in the previous Office Action and as such this claim is also believed to be in condition for allowance.

Claim 21 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Schindler in view of Malladi and in further view of Datari. Applicant respectfully reasserts the relevant remarks made above with respect to Schindler however the claim requires that the same frame buffer store for example one line of frame buffer memory of pixel information of a video image to be displayed wherein a second mode of operation compressed transport stream data stored in the frame buffer wherein one line of the frame buffer memory is representative of one transport stream packet. Such a method does not appear to be taught by the combination of the references

since it appears that the references do not include the teachings alleged in the Office Action and do not appear to provide any motivation for their combination.

For example, the Office Action cites Schindler as teaching that in a second mode of operation, Schindler stores the compressed transport stream in the same frame buffer that pixel information is stored in. However, Applicants are unable to find the teachings where the frame buffer that stores the compressed transport stream and that also stores the pixel information is a frame buffer of a video adapter. If the rejection is maintained, Applicants respectfully a showing as to what element the Office Action alleges teaches a second mode of operation and which element is the alleged frame buffer in a video graphics adapter. As noted above Applicants respectfully submit that Schindler does not describe a video graphics adapter as claimed but to the contrary a video graphics adapter card wherein the compressed video is stored in the frame buffer memory. In fact the video RAM 518 in Schindler only appears to store video signal information as noted for example in col. 11, lines 49-53.

Moreover, Schindler does not describe, as admitted by the Office Action, the storing of the compressed video. Moreover, the Office Action appears to cite a different memory name, namely memory 514 as the alleged memory that stores the compressed transports stream. As noted in the reference, DRAM 514 stores data, however this frame buffer does not store the pixel information as required by the claim and as such Schindler teaches a different structure than that claimed. Accordingly, this claim is also believed to be in condition for allowance for this reason.

Accordingly, Applicants respectfully submit that the claims are in condition for allowance and that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

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